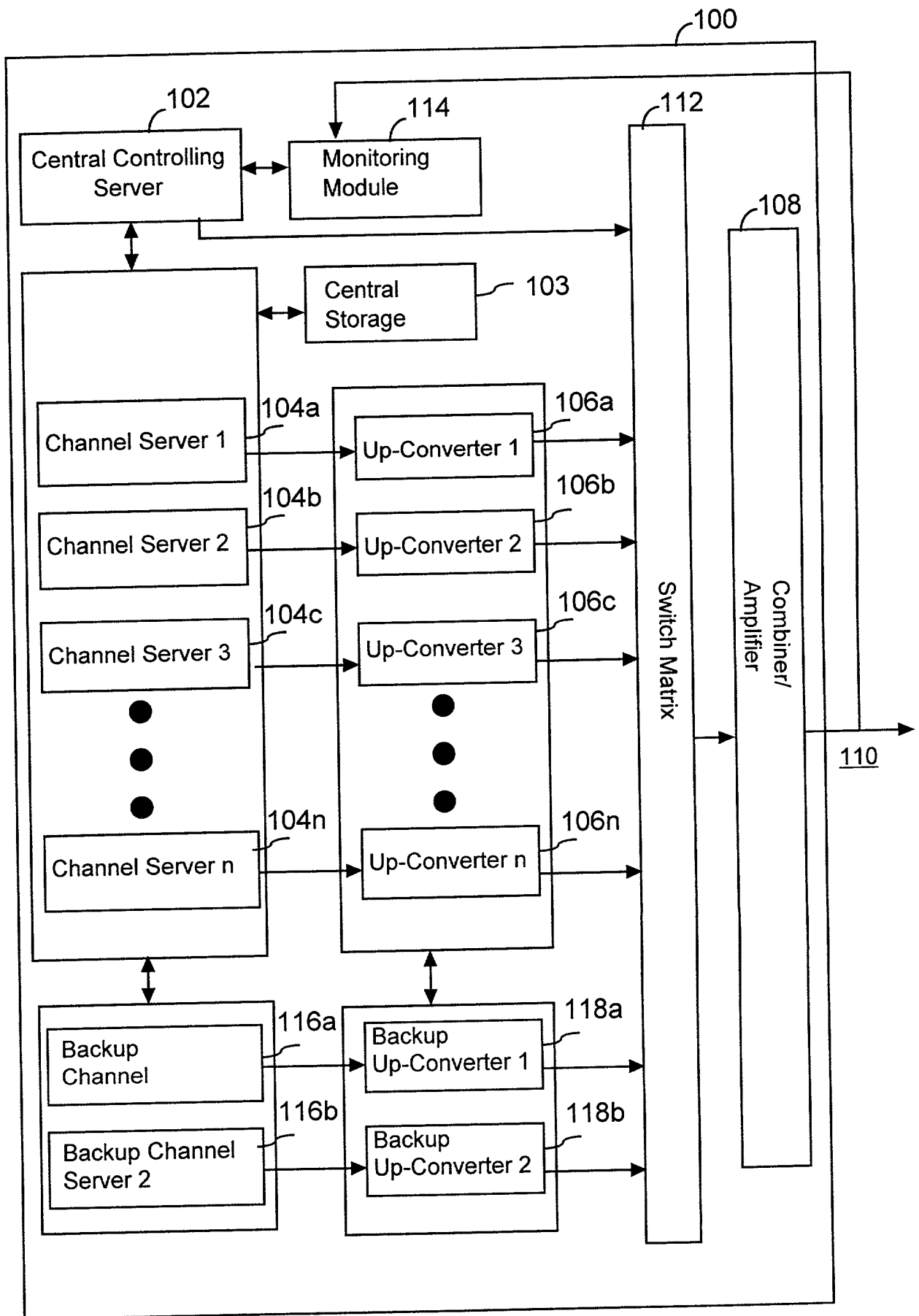
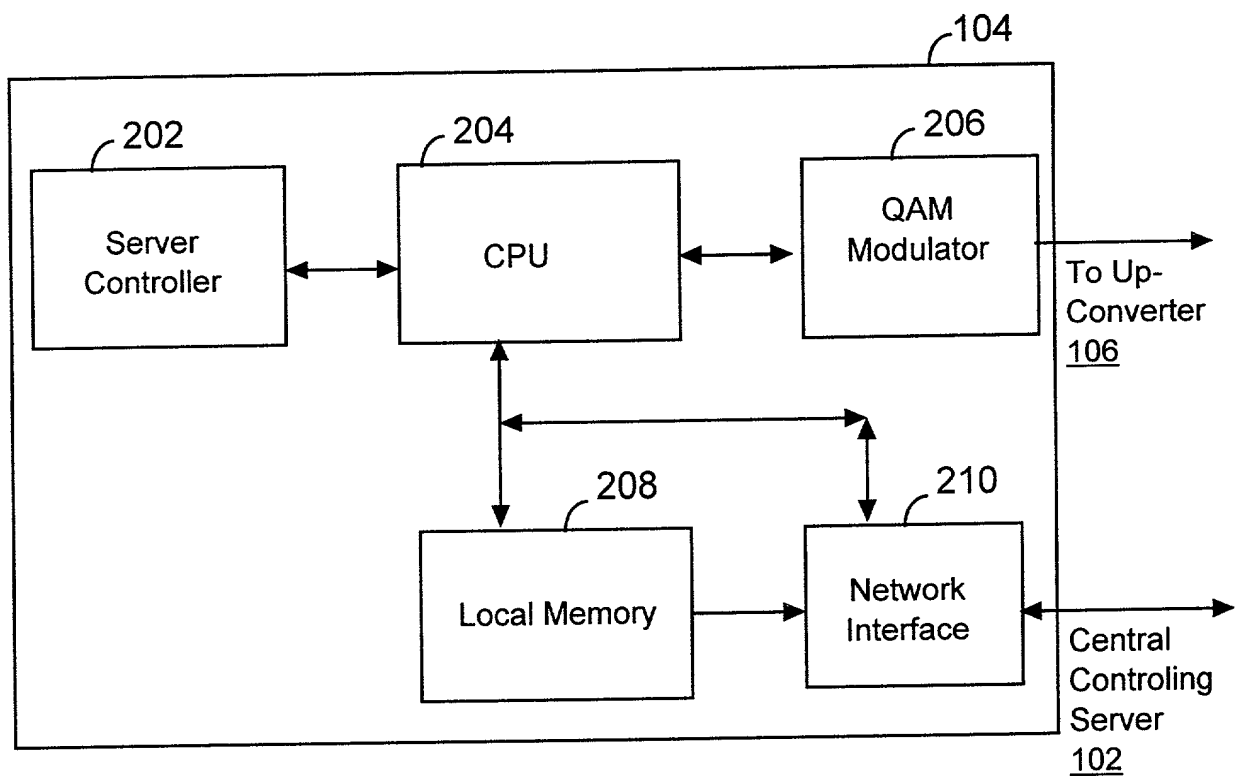


FIG. 1A



**FIG. 1B**



**FIG. 2**

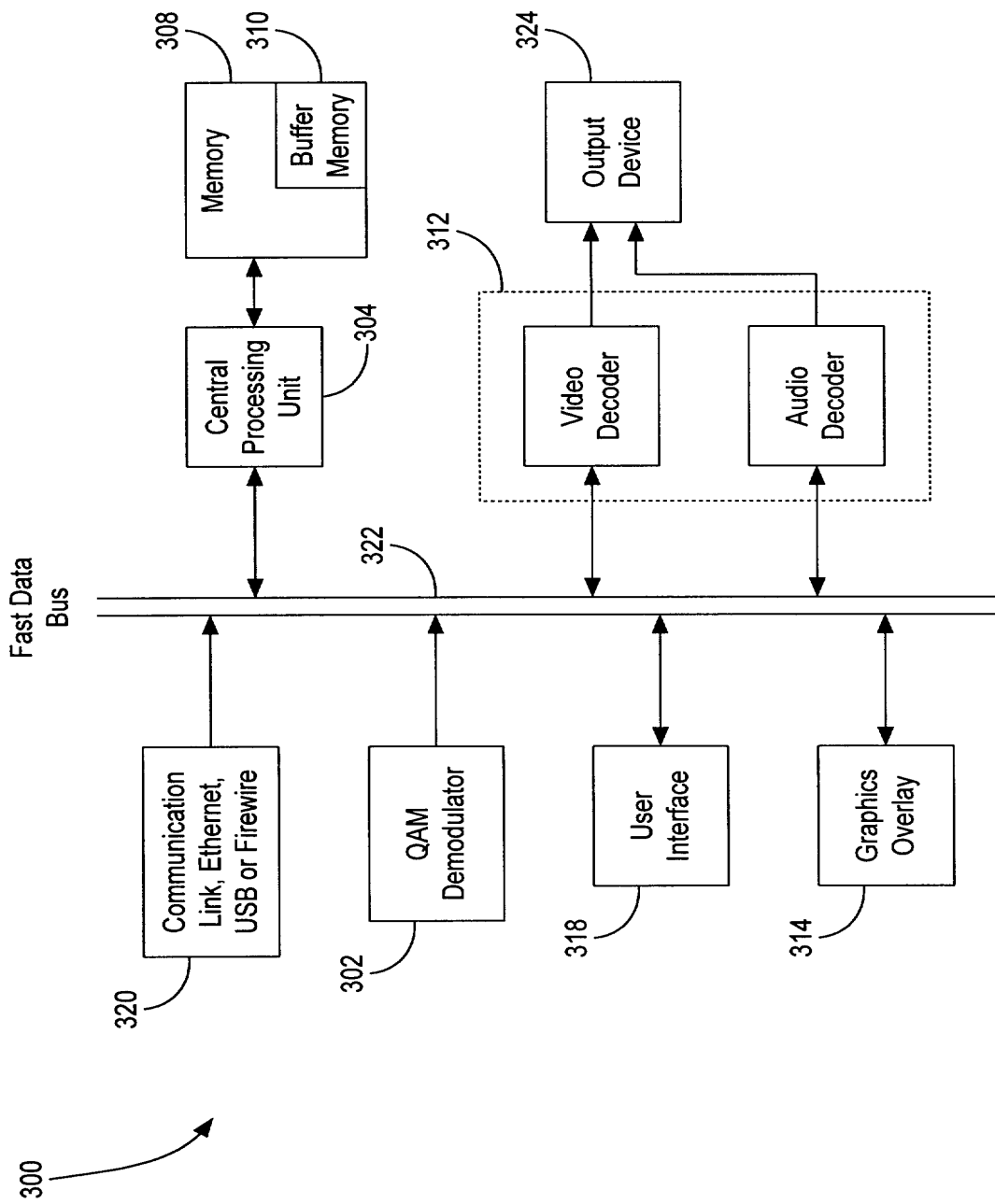
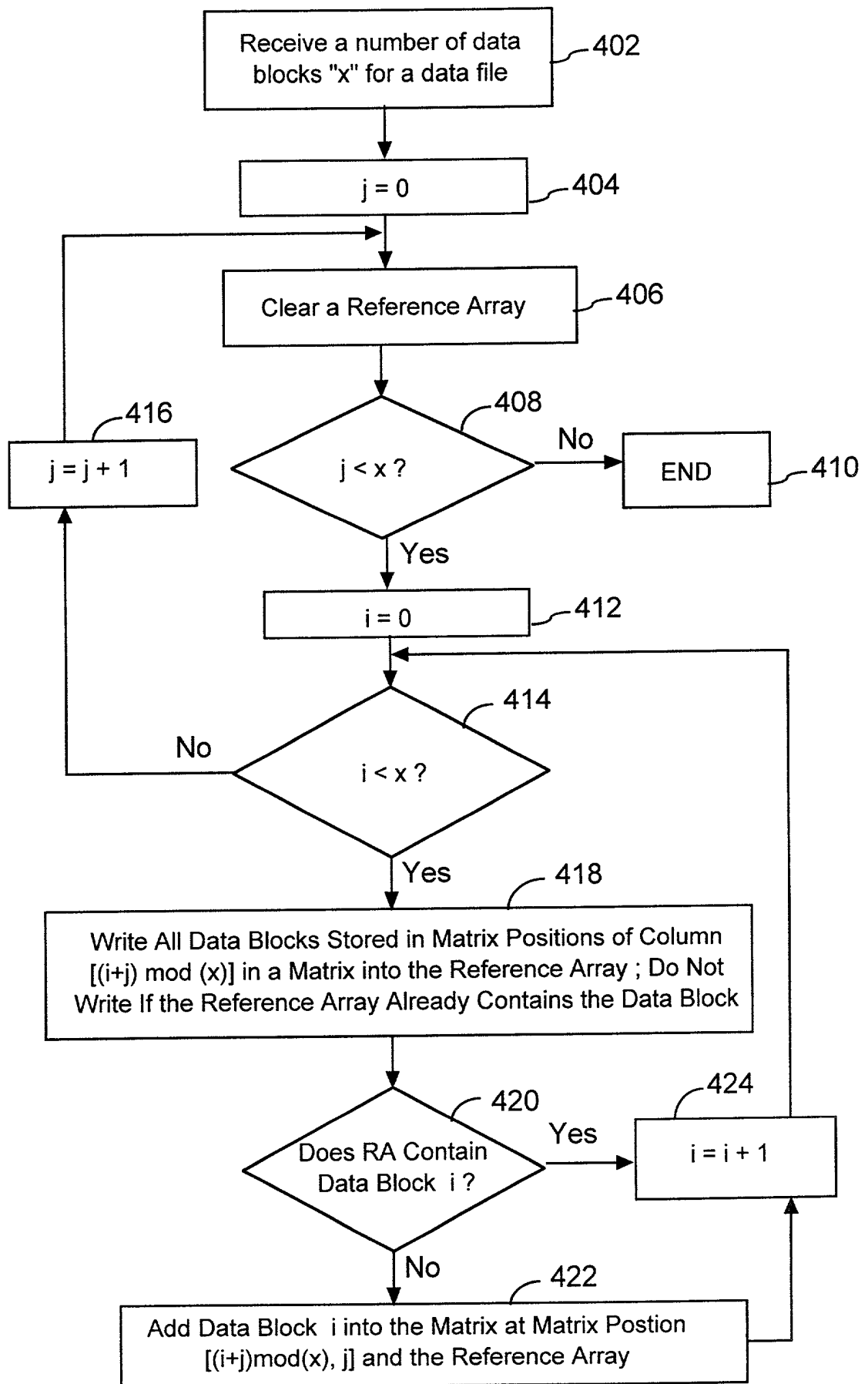


FIG. 3



**FIG. 4**

Time Slot	Bandwidth			
TS0	blk0	<-->	<-->	<-->
TS1	blk0	blk1	blk3	<-->
TS2	blk0	blk2	<-->	<-->
TS3	blk0	blk1	blk3	blk4
TS4	blk0	blk4	<-->	<-->
TS5	blk0	blk1	blk2	blk5

**FIG. 5**  
Scheduling Matrix

Time Slot	Bandwidth			
TS0	blk0	blk0	blk1	blk3
TS1	blk0	blk2	blk0	blk1
TS2	blk3	blk4	blk0	blk4
TS3	blk0	blk1	blk2	blk5
TS4				
TS5				

**FIG. 6**  
Scheduling Matrix with Idle Bandwidth Filled

Time Slot	Bandwidth			
TS0	blk0	blk0	blk1	blk3
TS1	blk0	blk2	blk0	blk1
TS2	blk3	blk4	blk0	blk4
TS3	blk0	blk1	blk2	blk5

**FIG. 7**  
New Reduced Idle Bandwidth Scheduling Matrix

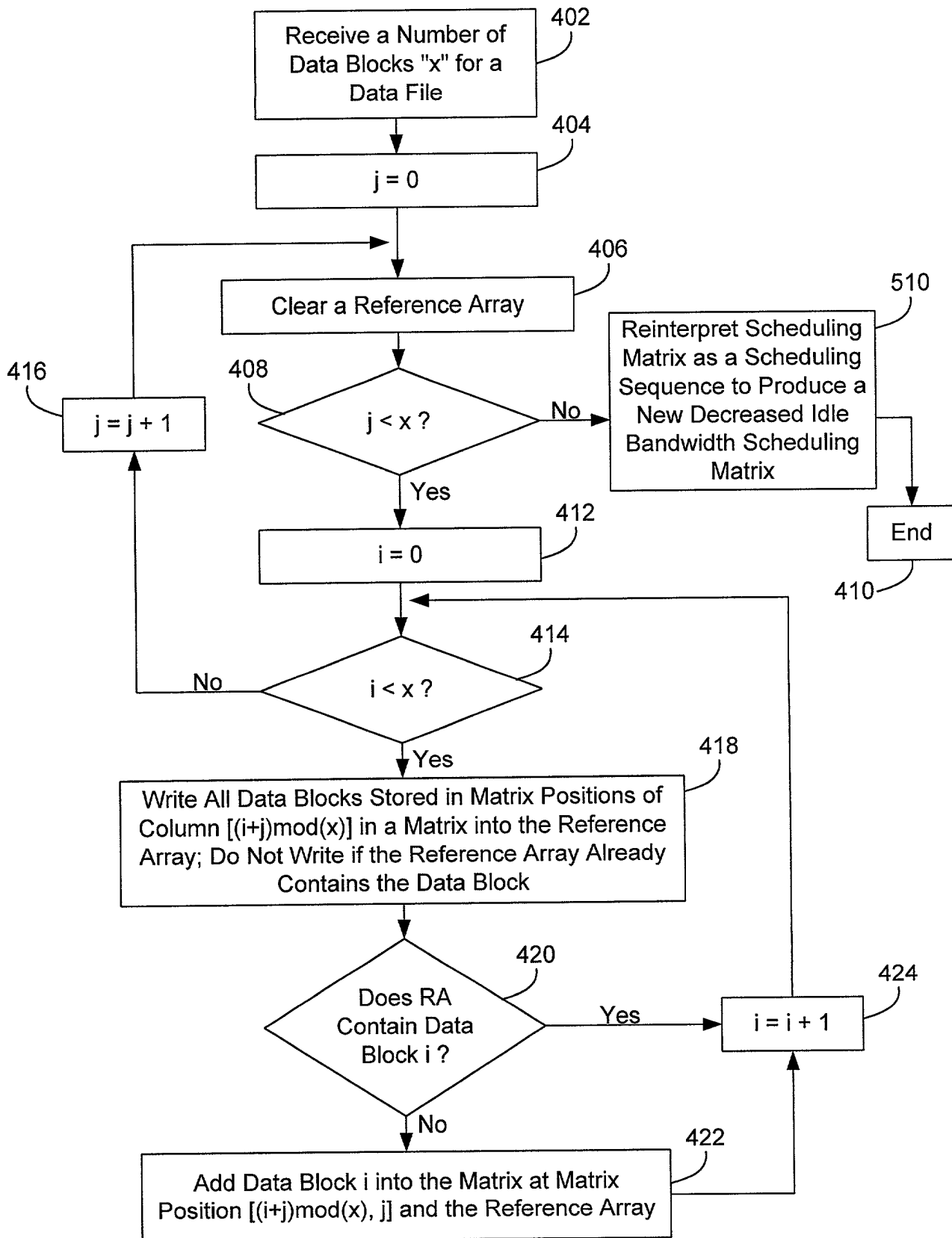


FIG. 8

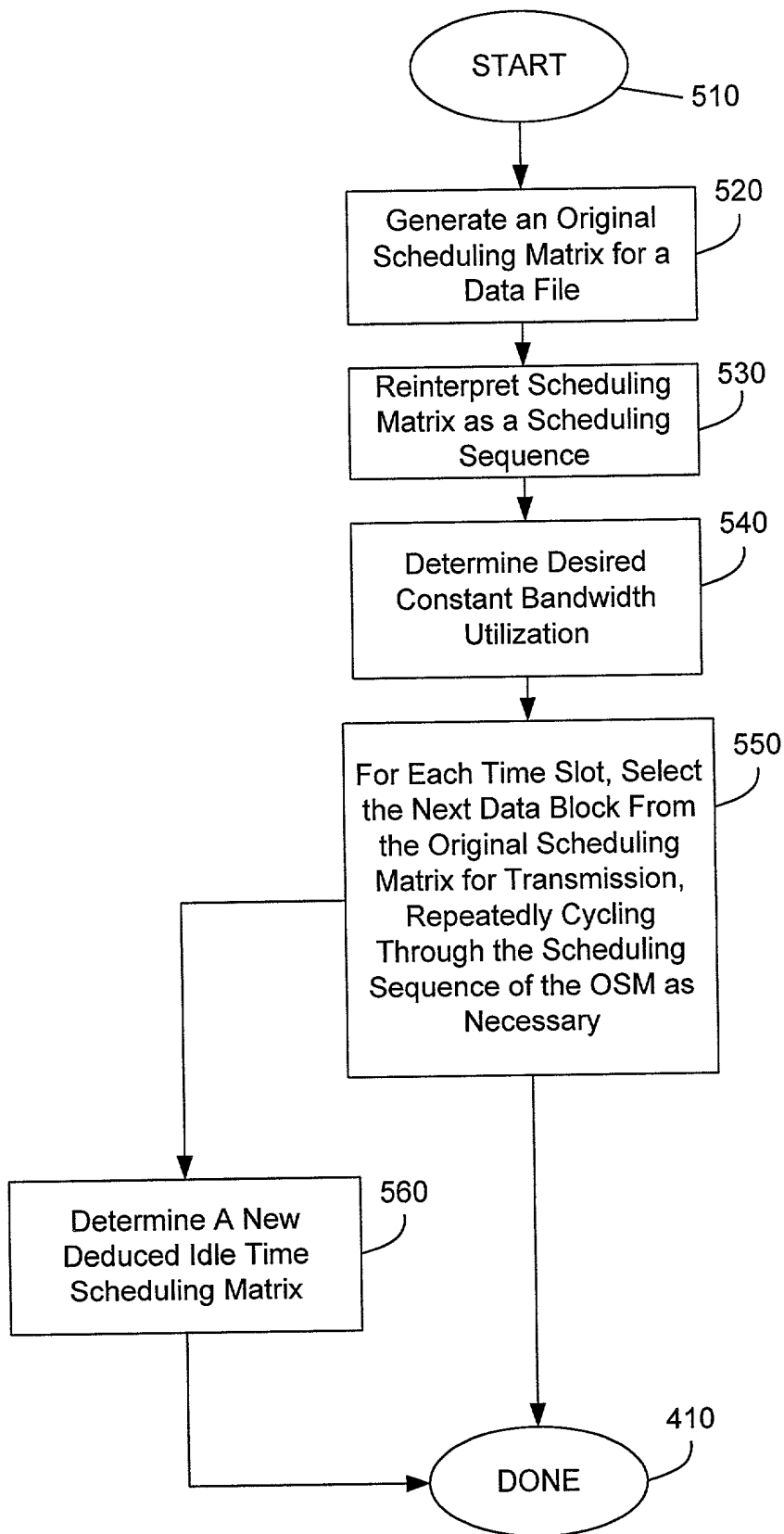


FIG. 9



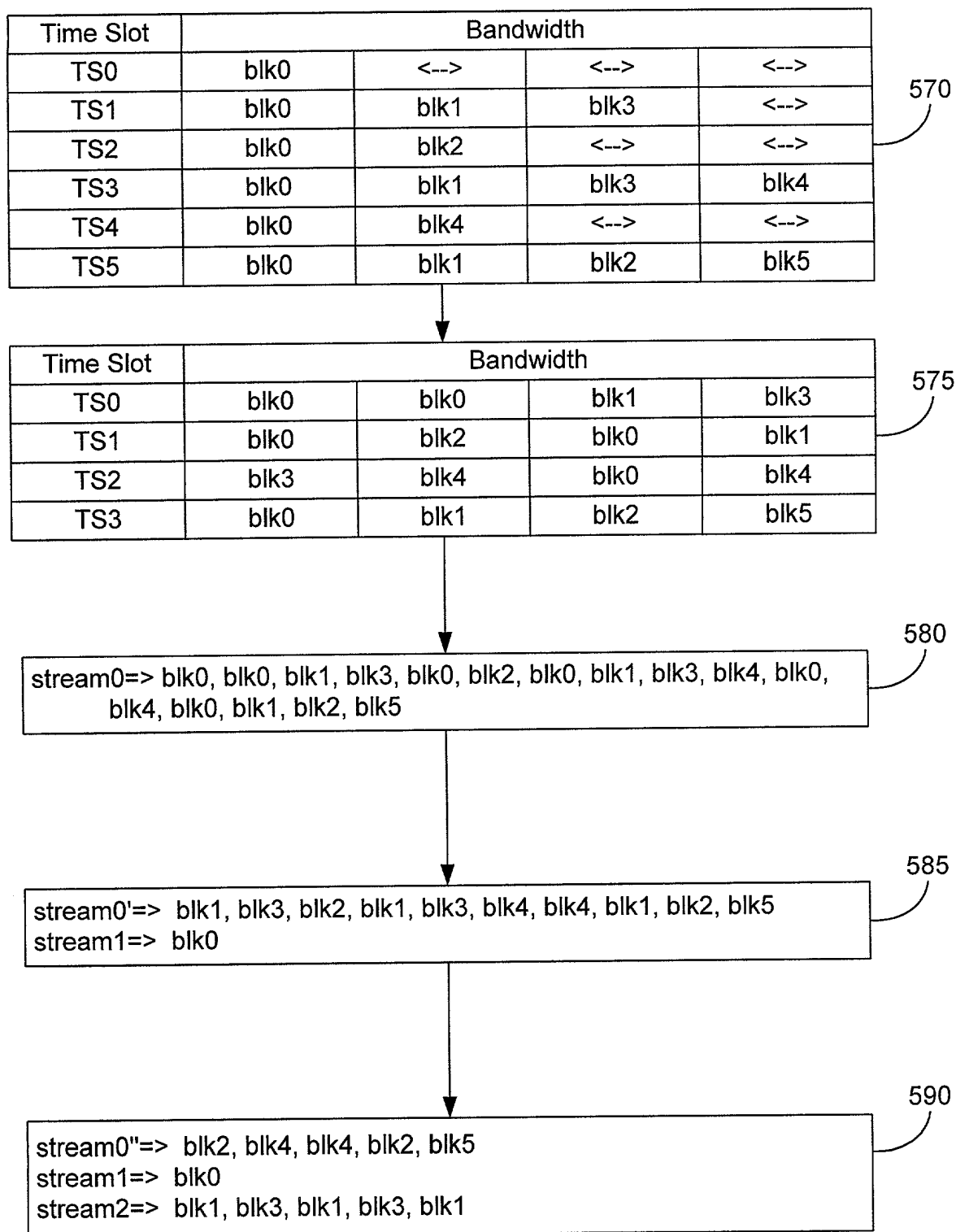


FIG. 10